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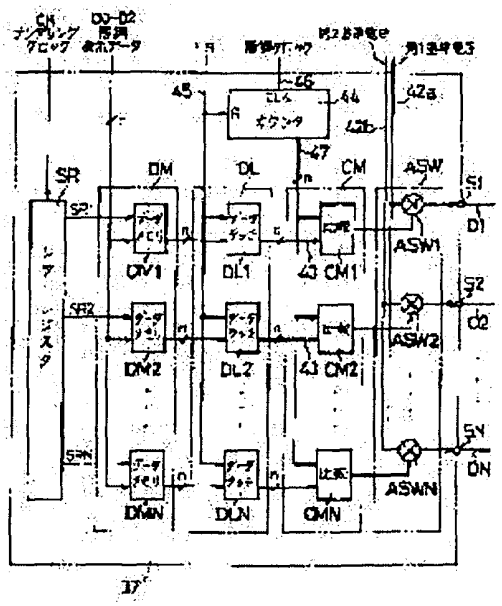
(54) DRIVING METHOD FOR DISPLAY PANEL AND DEVICE THEREFOR

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the number of connecting terminals of the source driver which drives an active matrix type liquid crystal display panel and to reduce the number of analog switches of the source driver.

SOLUTION: Voltages, which increase with time, are respectively supplied to each of source lines O1 to ON through analog switches ASW. One of the inputs of comparator circuits CM is given gradation display data for each of the source lines O1 to ON during one horizontal scanning period. The other inputs are provided with the counted values of a gradation clock signals CLK generated during one horizontal scanning period by a counter 44. If the counted values are less than the values corresponding to gradation display data D0 to D2, the switches ASW are closed. If the counted values reach to the corresponding values, the switches ASW are opened. Thus, the voltages corresponding to the data D0 to D2 are charged/discharged to



and from picture element electrodes and are held.

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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the method and equipment for driving display panels, such as for example, an active-matrix form liquid crystal display panel.
[0002]
[Description of the Prior Art] The 1st advanced technology which is typical advanced technology is shown in drawing 17 . The source lines O1-ON and the gate lines L1-LM are formed in the active-matrix form liquid crystal display panel 11 which constitutes display 10 in the shape of a matrix, TFT T is arranged in the intersection position, respectively, and the voltage of the source lines O1-ON is alternatively given to the picture element electrode P through Transistor T.
[0003] The source lines O1-ON are connected to the source driver 12 constituted by the semiconductor integrated circuit. The source driver 12 gives any one voltage of a total of eight kinds of reference voltages V0-V7 supplied to each source line Ok (k=1-N) from the source 13 of reference voltage according to the indicative datas D0-D2 which consist of the triplet which corresponds individually to the source lines O1-ON through Terminals S1-SN. The gate driver 14 which consists of a semiconductor integrated circuit outputs gate signals G1-GM to the gate lines L1-LM. The source driver 12 is 1 horizontal scanning period, and gives the reference voltage based on the indicative datas D0-D2 matched with each picture element electrode P's to which each gate signal Gj (j=1-M) is given to the source line Ok, respectively.
[0004] Drawing 18 is the block diagram showing concretely the composition of a part of source driver 12 of the 1st advanced technology shown in drawing 17 . The source driver 12 equips each source lines O1-ON with the decoder circuit FRk (k=1-N) which corresponded individually, answers the data d0-d2 corresponding to indicative datas D0-D2, respectively, gives eight kinds of reference voltages V0-V7 from the source 13 of reference voltage alternatively to the source line Ok through analog switches ASW0-ASW7, and displays eight gradation.
[0005] In the 1st advanced technology shown in such drawing 17 and drawing 18 , the individual reference voltages V0-V7 corresponding to each gradation are given from the source 13 of reference voltage in the source driver 12. The end-connection child for each reference voltages V0-V7 being given is [being the number of reference voltages, and / same number] necessary, and since reference voltage is further outputted in the source driver 12, the analog switches ASW0-ASW7 which correspond individually are needed for each gradation at the source driver 12.
[0006] The analog switches ASW0-ASW7 in the source driver 12 need to make the on resistance low enough, in order to write in correctly the level of the reference voltages V0-V7 chosen as the source lines O1-ON of the display panel 11 connected to the exterior of the source driver 12. Therefore, generally the area occupied within the semiconductor chip of analog switches ASW0-ASW7 is the need about ten times to about dozens times compared with the logical circuit element by which ON/OFF control is carried out for the logical operation in the source driver 12.
[0007] The rate for which it accounts to the whole area in which the semiconductor chip set of the

source driver 12 is formed of the above reasons has large analog switches ASW0-ASW7. Therefore, the increase in the number of the analog switches ASW0-ASW7 by the formation of many gradation brings a result which leads to increase of the size of a semiconductor chip as it is.
[0008] In recent years, although the device for miniaturizing a chip size in semiconductor chip sets, such as the source driver 12, is performed, there is a limit in miniaturizing the terminal itself and to decrease the number of end-connection children is desired. Furthermore, to decrease the number of the analog switches ASW0-ASW7 contained in the source driver 12, for example, to miniaturize the chip size of the source driver 12 which consists of a semiconductor integrated circuit, and to plan cost reduction is desired.
[0009] In the 1st advanced technology, in performing 16 gradation displays, for example using a 4-bit indicative data, the end-connection child for the reference voltage which generates 16 kinds of voltage is needed, and it needs a total of 16 analog switches corresponding to each of that reference voltage further. In practice, mass-production-ization of the source driver 12 for performing much more gradation displays of 64 gradation, 256 gradation, etc. has resulted in the situation of being impossible.
[0010] The advanced technology which makes it possible to decrease the number of end-connection children of reference voltage, and to decrease the number of analog switches as the 2nd advanced technology, and to miniaturize a semiconductor chip is indicated by JP,4-214594,A. The composition which the display currently indicated by the aforementioned official report simplified is shown in drawing 19 .
[0011] The switching element 19 which is formed in the intersection position of the picture element electrode 16, the drain line 17, the gate line 18, and the these drain lines 17 and the gate line 18 among the substrates of the couple which intervenes liquid crystal at one substrate, and gives the voltage of the drain line 17 to the picture element electrode 16 is formed, and the data electrode 20 for every train prolonged in the upper and lower sides of drawing 19 is formed in the substrate of another side.
[0012] A control pulse is given to the gate line 18, it scans by the scanning circuit 21, and the criteria gradation signal with which voltage changes at a fixed rate is impressed to the picture element electrode 16 through the drain line 17 within each of this horizontal scanning period. That is, the voltage of the lamp wave to which voltage rises or descends with time within 1 horizontal scanning period from the single criteria gradation signal circuit 23 is given to the drain line 17 in common. A voltage level is decided in the data electrode 20, and only the period corresponding to the gradation level supplies the data signal which will be in a high impedance state during residual to it from the data signal supply circuit 22. That is, in the data electrode 20, the voltage on which a voltage level decides only the time according to gradation level is given, and gradation level is adjusted with the length of the period which the voltage level of a data electrode has decided in this way.
[0013] In the 2nd above-mentioned advanced technology, there is a big problem that it is necessary to form the data electrode 20 of a large number divided for every train in the substrate of aforementioned another side. The aforementioned another side substrate which counters the picture element electrode 16 of the liquid crystal display panel generally used widely now has the single common electrode formed over the whole picture element electrode 16 of these large number. Therefore, since it is necessary to redesign the display panel itself newly in carrying out the advanced technology concerned, operation of the advanced technology concerned is difficult.
[0014] Moreover, in this 2nd advanced technology, since gradation level is held at the data electrode 20 side, there is a problem that the auxiliary capacity for data-hold currently formed in aforementioned one substrate of a display panel used for general from the former cannot be used as it is.
[0015] Moreover, the 3rd advanced technology is indicated by JP,5-297833,A and the composition which the advanced technology concerned simplified is shown in drawing 20 . The data for written-in one line will be transmitted to the data latch circuit 29 in parallel, and a shift register 27 will hold it, if the timing which writes the input data constituted, respectively in a data register 28 is controlled by 4 bits based on a clock signal CLK to each colors R and G and every B and the input data for one line is written in a data register 28.
[0016] The data held by the data latch circuit 29 are supplied to a comparator 30 to predetermined

timing. In a comparator 30, the data from the data latch circuit 29 and the counted value which consists of 4 bits from the 4-bit counter 31 are compared with each colors R and G and every B, and a comparison result is supplied to the sample hold circuit 32 with a built-in selector. The stair-like wave voltage VR and VB from which level changes, respectively in predetermined eight stages and two stages of the stair-like wave potential circuits 33 and 34 other than the comparison result of a comparator 30 is supplied to the sample hold circuit 32 with a built-in selector.

[0017] The sample hold circuit 32 with a built-in selector carries out sample hold of the signal of the level from the stair-like wave voltage generation circuits 33 and 34 according to the comparison result of a comparator 30 by the capacitor for sample hold in which it is built by the sample hold circuit 32 with a built-in selector. Voltage VDD is supplied to the output buffer 35, and the signal level according to the charge voltage level charged by the aforementioned capacitor in the sample hold circuit 32 with a built-in selector is outputted to each colors R and G and every B, and is given to the line for every train.

[0018] In this 3rd advanced technology, it has the capacitor for sample hold in the sample hold circuit 32 with a built-in selector, and the potential by the charge accumulated at the capacitor is outputted at voltage HOROA by the operational amplifier for every line in which it was prepared in the output buffer 35. Therefore, the output of the stair-like wave voltage generation circuits 33 and 34 does not have composition which is only given to the capacitor of the sample hold circuit 32 with a built-in selector, and is directly given to the line of a display panel. Since the voltage given to each line of a display panel is the voltage amplified by the operational amplifier prepared in the output buffer 35, by dispersion in the property of an operational amplifier, the voltage given to each line changes to un-wanting, and causes deterioration of display grace. The output voltage range by that the deflection of the output voltage resulting from dispersion in input offset voltage exists and limit of the dynamic range of the operational amplifier depends dispersion in the property of this operational amplifier on a bird clapper etc. narrowly.

[0019] Furthermore, JP,7-50389,B is indicated as 4th advanced technology. Drawing 21 is the block diagram showing the composition of the X driver 120 for a source electrode drive indicated by the aforementioned official report, and drawing 22 is the timing chart of each signal in the X driver 120.

[0020] A shift register 121 controls the timing which writes the 4-bit data input signals PD1-PD4 in four half latches 129 of the latch A circuit 122 based on a start pulse XSP and a clock signal XCL. M sets of four half latches 129 are formed in the latch A circuit 122, if data are held at M sets of half latches 129, latch clock signal LCL shown in drawing 22 (3) will be inputted into the half latch 130 of the latch B circuit 123, and the aforementioned data will be held.

[0021] The 4-bit binary counter 124 is reset by latch clock signal LCL, and carries out counting of the basic signal F16 for gradation shown in drawing 22 (2). Output QA-QD of a binary counter 124 and the output of the aforementioned half latch 130 are inputted into M comparators 138 of a comparator 125, and a comparison result is given to the input D of D flip-flop 126 as an output signal Y shown in drawing 22 (4). D flip-flop 126 incorporates the output of a comparator 138 synchronizing with the start of the aforementioned basic signal F16 for gradation, is set by latch clock signal LCL, and is reset by stop signal STOP. The output of D flip-flop 126 can be pulled up to the voltage which can drive an analog switch 128 by the level shifter 127.

[0022] The video voltage VID shown in drawing 22 (1) is supplied to the analog switch 128, and opening and closing are controlled by the output of a level shifter 127. The primary video voltage VID changes from the voltage VOFF of the off-level of liquid crystal linearly to the voltage VON of on-level in 1 horizontal scanning period TH.

[0023] The video voltage VID which changes as mentioned above is that opening-and-closing control of the analog switch 128 is carried out, and is impressed to the pixel electrode of a liquid crystal display panel through a source signal line as voltage VPIX shown in drawing 22 (6). As for voltage VPIX, the level of the time ta when the gradation basic signal F16 after an output signal Y falls starts is held till the time tb which the horizontal scanning period TH ends.

[0024] In this 4th advanced technology, since the video voltage VID supplied to a source electrode through an analog switch 128 serves as a saw wave linear the 1st order, when the timing of the output

signal of a comparator circuit 138 shifts delicately, the voltage of the timing concerned will be held and deterioration of display grace is caused.
[0025]
[Problem(s) to be Solved by the Invention] The purpose of this invention is offering the drive method of a display panel and equipment which reduce the number of end-connection children, and the number of analog switches, attaining many gradation-ization, and enabled it to enable miniaturization of semiconductor chips, such as a source driver, reduction in the consumed electric current, low-cost-izing, high-density-assembly-ization, etc. by this.
[0026] Other purposes of this invention are offering the drive method of the display panel which uses the display panel in which the picture element electrode of a large number which while is used widely now and prepared in the substrate, and the common electrode single to the substrate of another side which counters through dielectric layers, such as liquid crystal, were formed as it is, and enabled it to reduce the number of end-connection children, and the number of analog switches as mentioned above moreover, and equipment.
[0027] The purpose of further others of this invention is offering the drive method of the display panel which enables it to prevent deterioration of the display grace by dispersion in the property of such a semiconductor device, and enabled it to aim at miniaturization of semiconductor chips, such as a source driver, and reduction of power consumption, and equipment, without using complicated circuitry, such as an operational amplifier like the advanced technology described in relation to above-mentioned drawing 20 .
[0028]
[Means for Solving the Problem] this invention is the drive method of the display panel characterized by generating periodically the voltage which changes gradually with time progress, impressing the aforementioned voltage at the time of passing the time corresponding to the gradation indicative data to an electrode for every aforementioned period, and making it hold by the inter-electrode dielectric layer in the drive method of the display panel which impresses voltage to inter-electrode [of the couple which intervenes a dielectric layer], and performs a gradation display. Moreover, this invention is set to the drive method of the display panel which impresses voltage to inter-electrode [of the couple which intervenes a dielectric layer], and performs a gradation display. When the voltage which changes gradually with time progress is generated periodically and the aforementioned voltage reaches the value corresponding to the gradation indicative data for every aforementioned period, it is the drive method of the display panel characterized by impressing the voltage of the value to an electrode and making it hold by the inter-electrode dielectric layer.
If this invention is followed, the voltage which follows on time progress, and rises or descends gradually will be generated periodically, voltage when voltage and the aforementioned voltage when the time corresponding to a gradation indicative data passes reaches the voltage value corresponding to the gradation indicative data will be impressed to the electrode of a display panel, and a gradation display will be performed. Therefore, a multi-gradation display can be performed without making the number of the switching elements for impressing voltage to the terminal and electrode into which voltage is inputted increase, and the miniaturization of the composition of display can be attained. Moreover, since the number of the switching elements for impressing voltage to an electrode can be reduced performing a multi-gradation display, the miniaturization of a semiconductor chip can be attained and low-power-izing of a semiconductor chip, low-cost-izing, high-density-assembly-ization, etc. can be enabled.
If this invention is furthermore followed, this invention can be carried out using the ordinary display panel which has the another side substrate in which the single common electrode which while has many picture element electrodes, and intervenes and counters a substrate in a dielectric layer was formed as it is, and operation of this invention is very easy. Moreover, lines, such as a source line to which TFT (abbreviated name TFT), such as a metal oxide-film field-effect transistor (abbreviated-name MOS-FET) which is a picture element switching element in an active form matrix display panel, is connected in this ordinary display panel, respectively, Only one auxiliary capacity is formed in aforementioned one substrate between the gate lines of the point of a time sequential scanning direction rather than the gate

line to which the gate of each of that TFT is connected. Also in the composition which increases the capacity of the picture element electrode connected to TFT, and enabled it to hold the voltage corresponding to gradation level, this invention can be carried out as it is and is convenient. If this invention is followed, complicated circuits, such as an operational amplifier which was described in relation to the above-mentioned advanced technology, are not needed, but also by this, the miniaturization of a semiconductor chip can be attained and low-power-ization can be attained. In this invention, although the dielectric layer in a display panel is made into liquid crystal material and can be cooked, it may be for example, electroluminescence (abbreviated name EL) material as other dielectric layers, and the other materials may be used. Moreover, if this invention is followed, it is also possible to carry out in relation to the so-called simple matrix type display panel which countered in the active-matrix liquid crystal display panel using picture element switching elements, such as TFT (abbreviated name TFT), etc. in the shape of [which intervenes this invention not only being carried out but a dielectric layer] a matrix, and has been arranged, and even if it relates to the display panel which has other composition, this invention can be carried out again.

[0029] this invention is the period beforehand defined in the drive method of the display panel which impresses voltage to inter-electrode [of the couple which intervenes a dielectric layer], and performs a gradation display. The 1st voltage which rises gradually from the 1st potential to the 2nd potential with time progress, The 2nd voltage which descends from the 2nd potential to the 1st potential is created, and change ****** of the 1st voltage and 2nd voltage is carried out for every aforementioned period. to one electrode The above 1st at the time of passing the time corresponding to the gradation indicative data or the 2nd voltage is impressed for every aforementioned period. to the electrode of another side It is the drive method of the display panel characterized by impressing the 2nd potential when the 1st potential is impressed when the 1st voltage is impressed to aforementioned one electrode, and the 2nd voltage is impressed, and making it hold by the inter-electrode dielectric layer. Moreover, this invention is set to the drive method of the display panel which impresses voltage to inter-electrode [of the couple which intervenes a dielectric layer], and performs a gradation display. The 1st voltage which rises gradually with time progress from the reference voltage defined beforehand the period defined beforehand, The 2nd voltage which descends gradually with time progress from the reference voltage defined beforehand is created, and the 1st and 2nd voltage is switched and outputted for a number of every periods defined beforehand. the account of before -- to one electrode The reference voltage defined beforehand is impressed. the 1st and the 2nd voltage at the time of passing the time corresponding to the gradation indicative data through each signal line prepared in order to impress voltage to the electrode concerned -- respectively -- alternation -- impressing -- the electrode of another side -- the account of before -- It is the drive method of the display panel characterized by making it hold by the inter-electrode dielectric layer. If this invention is followed, the voltage to which the elevation to the 2nd potential or the descent to the 2nd potential [1st] from potential switches from the 1st potential gradually with time progress will be generated periodically, and the voltage corresponding to a gradation indicative data will be impressed to one electrode of a display panel. When the aforementioned voltage rises, the 1st potential is impressed to the electrode of another side, and the 2nd potential is impressed when descending. Voltage is made to hold to the dielectric layer which exists between one electrode and the electrode of another side. Therefore, the voltage generated by the equipment which drives one electrode at the aforementioned periodic target can be supplied, many gradation can be displayed in alternating current by impressing the 1st or 2nd voltage to the electrode of another side alternatively, and the number of the terminals for a reference voltage input prepared in the aforementioned driving gear can be decreased compared with the conventional driving gear which displays the same gradation. Moreover, the 1st voltage which rises gradually with time progress from the reference voltage beforehand defined the period defined beforehand as the method of an alternating current drive and the 2nd voltage which descends gradually The method of switching for a number of every periods defined beforehand, supplying each signal line prepared in order to impress voltage to aforementioned one electrode, impressing the voltage in the time corresponding to the gradation indicative data to aforementioned one electrode, and displaying by impressing reference voltage to the electrode of another side may be used.

[0030] this invention generates on a target the gradation clock signal of the number more than the number of gradation which should indicate by gradation one by one time for every aforementioned period, carries out counting of this gradation clock signal, and is characterized by impressing the voltage at the time of an enumerated data turning into a value corresponding to the gradation indicative data to an electrode, and making it hold. If this invention was followed, when it will carry out counting of the gradation clock signal generated more than the number of gradation in each period and the enumerated data concerned will turn into a value corresponding to the gradation indicative data, the voltage changed on the aforementioned periodic target is impressed to an electrode. Therefore, the voltage corresponding to a gradation indicative data can be certainly impressed to an electrode, and the gradation display based on the aforementioned gradation indicative data can be performed.
[0031] In the driving gear which this invention impresses the voltage supplied to a display panel equipped with the electrode of the couple which intervenes a dielectric layer from a voltage source, and performs a gradation display The switching element for voltage impression which controls the voltage impressed to the aforementioned electrode, A gradation indicative-data generating means defined beforehand to generate a gradation indicative data for every period, Each output with a means is answered. the time check which clocks time for every aforementioned period -- a means, a gradation indicative-data generating means, and a time check -- The switching control means which turns on or controls [OFF] the switching element for voltage impression is included. to the aforementioned switching element for voltage impression It is the driving gear of the display panel characterized by giving the voltage to which a voltage source follows on the time progress which makes it generate for every aforementioned period, and goes up or descends gradually. If this invention is followed, the voltage which follows for example, on time progress, and rises or descends gradually will be generated from a voltage source for every periods, such as a display panel, for example, 1 horizontal scanning period etc., and it will give the switching element for voltage impression. the time corresponding to the gradation indicative data generated from a gradation indicative-data generating means for every period -- a time check -- a means -- clocking -- a gradation indicative-data generating means and a time check -- the switching element for voltage impression is controlled by the switching control means, and the voltage corresponding to a gradation indicative data is impressed to the electrode of a display panel, and is made to answer an output with a means and to hold Therefore, by controlling the switching element for voltage impression by timing corresponding to the gradation indicative data, the gradation display based on a gradation indicative data can be performed on the voltage which changes gradually, and the terminal for a reference voltage input prepared in the equipment which drives a display panel can be cut down. Moreover, it is prepared in a driving gear, for example, since one switching meanses for voltage impression, such as an analog switch, can supply the voltage corresponding to the gradation indicative data to an electrode if they are established, they can make small area in which a driving gear is formed. Furthermore, voltage is given to the picture element electrode for the voltage from a voltage source through the picture element switching element through lines, such as a source line of a display panel, through the switching element for voltage impression. Since voltage is given to electrodes, such as a picture element electrode, as it is and charge or electric discharge is performed, it becomes unnecessary that is, to be able to attain simplification of composition compared with the above-mentioned advanced technology, and to form the capacitor for sample hold etc. separately.
[0032] this invention -- a time check -- the gradation clock signal of the number more than the number of gradation which a means should carry out a gradation display into the period for every aforementioned period -- a time order -- with the gradation [degree] clock signal generating means generated-like When a switching control means becomes a value corresponding to the gradation indicative data from a gradation indicative-data generating means in the enumerated data of a counter including the counter which adds and carries out counting of the gradation clock signal, it is characterized by turning on or OFF controlling the switching element for voltage impression. Moreover, this invention is set to the driving gear which impresses voltage to a display panel equipped with the electrode of the couple which intervenes a dielectric layer, and performs a gradation display to it. A gradation indicative-data generating means defined beforehand to generate a gradation indicative data

for every period, A gradation clock signal generating means to generate on a target the gradation clock signal of the number more than the number of gradation which should indicate by gradation into the period one by one time for every aforementioned period, the time check containing the counter which adds and carries out counting of the gradation clock signal -- with a means The switching element for voltage impression which controls the voltage impressed to the aforementioned electrode, An output with a means is answered. the voltage which is based on the enumerated data of the aforementioned counter, and rises or descends gradually -- generating -- the aforementioned switching element for voltage impression -- giving -- a gradation indicative-data generating means and a time check -- It is the driving gear of the display panel characterized by including the switching control means which turns on or controls [OFF] the switching element for voltage impression. the voltage which will follow on the time progress supplied from a voltage source, and will rise or descend gradually if this invention is followed -- the switching element for voltage impression -- minding -- the electrode of a display panel -- impressing -- a gradation indicative-data generating means and a time check -- a flow/interception of the switching element for voltage impression is controlled by switching-control means to by_which an output with a means is given so that the voltage value corresponding to a gradation indicative data is impressed, and a gradation display is carried out to a display panel Therefore, the number of the terminals for a voltage input in a driving gear is [that the voltage supplied to a driving gear from a voltage source should just be voltage which changes to one kind of aforementioned stage target] reducible.

[0033] this invention is characterized by intercepting, when a switching control means presupposes that the switching element for voltage impression has been flowed when the enumerated data of a counter is under a value corresponding to a gradation indicative data and the enumerated data of a counter becomes beyond the value corresponding to a gradation indicative data. Moreover, this invention is characterized by only for time defining the switching element for voltage impression beforehand, when the enumerated data of a counter turns into a value corresponding to a gradation indicative data flowing through a switching control means, and making the voltage at the time of the flow hold to an electrode. The gradation [degree] clock signal generating means generated-like is included. moreover, this invention -- a time check -- the gradation clock signal of the number more than the number of gradation which a means should carry out a gradation display into the period for every aforementioned period -- a time order -- When a switching control means becomes the value which the enumerated data of a backward counter defines beforehand including the backward counter which the value corresponding to the gradation indicative data is set up, and is subtracted whenever it is reception of a gradation clock signal for every aforementioned period, It is characterized by turning on or OFF controlling the switching element for voltage impression. if this invention is followed -- a time check -- a means may be a counter which adds and carries out counting of the gradation clock signal which has a period shorter than the aforementioned period, or may be a backward counter subtracted from the enumerated data corresponding to a gradation indicative data a time check -- the voltage which changes gradually can be made to impress to a display panel certainly with the voltage value of the request corresponding to a gradation indicative data by answering the output of a means and controlling a flow/interception of the switching element for voltage impression

[0034] this invention is characterized by turning on or OFF controlling the switching element for voltage impression, when a switching control means becomes the value which the enumerated data of a backward counter defines beforehand including the backward counter which the value corresponding to the gradation indicative data is set up, and is subtracted whenever it is reception of a gradation clock signal for every aforementioned period. moreover, this invention -- a switching control means -- the switching element for voltage impression -- the enumerated data of a backward counter -- the account of before -- having flowed, when exceeding the value defined beforehand -- carrying out -- the enumerated data of a backward counter -- the account of before -- when it becomes below the value defined beforehand, it is characterized by intercepting moreover, this invention -- a switching control means -- the switching element for voltage impression -- the enumerated data of a backward counter -- the account of before -- when it becomes the value defined beforehand, it is characterized by only for time

setting beforehand flowing and making the voltage at the time of the flow hold to an electrode the enumerated data of a backward counter when following this invention and the switching element for voltage impression reaches the value corresponding to a gradation indicative data in the enumerated data of the aforementioned counter -- the account of before -- when the value defined beforehand, for example, zero, is reached, only time to set beforehand flows, and you may constitute so that the voltage at the time of the flow may be made to hold to electrodes, such as a picture element electrode [0035] this invention is characterized by a switching control means containing digital one/analog converter which generates the voltage which changes gradually based on the output of the aforementioned counter. this invention to moreover, the picture element electrode arranged in the 1st and the intersection position of the 2nd line which were arranged in the shape of a matrix, respectively The driver voltage given through the 1st line is given through the picture element switching element which flows with the picture element control signal to which it is given through the 2nd line. In the display panel which impresses the constant voltage used as criteria to the common electrode which counters a picture element electrode and is prepared, prepares the potential difference in the aforementioned picture element electrode and a common electrode, and performs a gradation display, and two or more horizontal scanning periods set beforehand The gate driver which makes it flow through the picture element switching element connected to the 2nd line to which the picture element control signal was given to the target one by one at each 2nd line, and the picture element control signal was given, during the aforementioned horizontal scanning period -- every -- with a gradation indicative-data generating means to derive the gradation indicative data in every line [the] on a target one by one by the serial bit The gradation indicative data from a gradation indicative-data generating means 1 horizontal scanning period every in a parallel bit The data latch circuit latched and derived, The voltage source which generates the voltage which follows on time progress, and rises or descends gradually for every horizontal scanning period, The switching element for voltage impression which intervenes between a voltage source and a picture element electrode, the time check which clocks the time in the horizontal scanning period for every horizontal scanning period -- a means, and a data latch circuit and a time check, when each output with a means is answered and the time corresponding to the gradation indicative data passes It is the display which turns on or controls [OFF] the switching element for voltage impression, and is characterized by including a switching control means to make voltage impress and hold to an electrode by this. this invention to moreover, the picture element electrode arranged in the 1st and the intersection position of the 2nd line which were arranged in the shape of a matrix The driver voltage given through the 1st line is given through the picture element switching element which flows with the picture element control signal to which it is given through the 2nd line. In the display panel which impresses the constant voltage used as criteria to the common electrode which counters a picture element electrode and is prepared, prepares the potential difference in the aforementioned picture element electrode and a common electrode, and performs a gradation display, and two or more horizontal scanning periods set beforehand The gate driver which makes it flow through the picture element switching element connected to the 2nd line to which the picture element control signal was given to the target one by one at each 2nd line, and the picture element control signal was given, during the aforementioned horizontal scanning period -- every -- with a gradation indicative-data generating means to derive the gradation indicative data in every line [the] on a target one by one by the serial bit The gradation indicative data from a gradation indicative-data generating means 1 horizontal scanning period every in a parallel bit The data latch circuit latched and derived, The switching element for voltage impression which controls the voltage supplied to a picture element electrode, A gradation clock signal generating means to generate on a target the gradation clock signal of the number more than the number of gradation which is going to indicate by gradation during [the] the horizontal scanning one by one time for every horizontal scanning period, When the counter which adds and carries out counting of the gradation clock signal, and the voltage which is based on the enumerated data of the aforementioned counter, and rises or descends gradually are generated, it gives the 1st aforementioned line and the time corresponding to the gradation indicative data passes It is the display which turns on or controls [OFF] the switching element for voltage impression, and is

characterized by including a switching control means to make voltage impress and hold to an electrode by this. If this invention is followed, counting of the gradation clock signal generated by the target one by one time will be added and carried out by the counter, it will create for every period which defines beforehand the voltage which is based on the enumerated data of a counter, and rises or descends gradually, and the voltage concerned will be impressed to the electrode of a display panel through the switching element for voltage impression. a gradation indicative-data generating means and a time check -- a flow/interception of the switching element for voltage impression are controlled by switching control means by which an output with a means is given so that the voltage value corresponding to a gradation indicative data is impressed, and a gradation display is performed to a display panel Therefore, since the reference voltage impressed to the electrode of a display panel is created within a driving gear in order to perform a gradation display, the terminal for a reference voltage input in a driving gear is reducible. It is made to flow through the switching element for voltage impression at the time of the start of for example, the aforementioned period, and when it becomes a voltage value corresponding to a gradation indicative data, it is made to intercept. Moreover, when it becomes a voltage value corresponding to a gradation indicative data, it is made to flow, and the aforementioned voltage is impressed, and you may make it make it intercept after impression of voltage. Furthermore, since the aforementioned voltage is voltage which synchronizes correctly and changes to a gradation clock signal gradually, in case a gradation display is performed, a desired voltage value can be correctly impressed to the electrode of a display panel. The time corresponding to the aforementioned gradation indicative data is equivalent to the value corresponding to the gradation indicative data of voltage which changes with time progress, if it puts in another way.

[0036]

[Embodiments of the Invention] Drawing 1 is the block diagram showing the composition of the liquid crystal display 100 for explaining the 1st gestalt of operation of this invention.

[0037] TFT (abbreviated name TFT) T (j, i) (j=1-M, i=1-N) whose active-matrix form liquid crystal display panel 36 the source lines O1-ON which are the 1st line at a M line N train, and the gate lines L1-LM which are the 2nd line are arranged on one substrate, and is a picture element switching element in those lines O1-ON and the intersection position of L1-LM is arranged.

[0038] TFT T by which the gate electrode is connected to the gate line Lj to which the gate signal Gj is given flows by giving a target gate signals G1-GM one by one at the gate lines L1-LM. The gradation display driver voltage from the source lines O1-ON is given to the picture element electrode P (j, i) by this through TFT T through which it has flowed, respectively.

[0039] The single common electrode Q which counters all these picture element electrodes P is formed in the substrate of another side which counters aforementioned one substrate through liquid crystal, and a gradation display is performed by the electric field between the common electrode Q and the picture element electrode P by which driver voltage is given to the aforementioned selection target. The voltage from which the aforementioned driver voltage and polarity differ on the basis of the voltage value defined beforehand is impressed to the common electrode Q. In addition, in drawing 1 , in order to show that the display for one picture element is performed by the picture element electrode P and the common electrode Q, the common electrode Q was divided and shown.

[0040] The source lines O1-ON are connected to the end-connection children S1-SN of the source driver 37 realized by the semiconductor integrated circuit, respectively. The gate lines L1-LM are connected to the end-connection children G1-GM of the gate driver 38 realized by the semiconductor integrated circuit, respectively. A reference mark with the same signal given to an end-connection child and its end-connection child into this specification may be attached and expressed.

[0041] In each horizontal scanning period WH when the gate lines L1-LM become high-level on a target one by one, TFT T which is the picture element switching element with which the gate electrode is connected to the high-level gate line Lj flows. Therefore, the driver voltage corresponding to the gradation indicative data given through the source lines O1-ON is charged in the liquid crystal layer which exists between the picture element electrode P and the common electrode Q. This charged voltage level is held during [when a total of M gate lines L1-LM is scanned] the 1 vertical scanning.

[0042] The gradation indicative datas D0-D2 of an in-series triplet are given to a target one by one from the display-control circuit 39 at the source driver 37 corresponding to each source lines O1-ON. The display-control circuit 39 generates clock signal creatine kinase and the latch signal LS, and gives them to the source driver 37 again. These reference marks D0-D2, and creatine kinase and LS may be used in order to show a signal, an end-connection child, or a line, and they are the same also about other reference marks in the following explanation.
[0043] The signal which synchronized with clock signal creatine kinase and the latch signal LS is also given to a gate driver 38 from the display-control circuit 39 through a line 40, and a gate driver 38 synchronizes and gives the sequential gate signals G1-GM to the gate lines L1-LM as mentioned above.
[0044] In order to give driver voltage to the source lines O1-ON, the source 41 of reference voltage is formed. This source 41 of reference voltage outputs the voltage which has the wave which increases gradually with the time progress shown in below-mentioned drawing 8 (4) through a line 42. The period of the voltage outputted from this source 41 of reference voltage is chosen equally to 1 horizontal scanning period WH.
[0045] Drawing 2 is the block diagram showing the concrete composition of the source driver 37, and drawing 3 is a wave form chart for explaining operation of the source driver 37 in 1 horizontal scanning period WH. You may be n= 3, when a reference mark n shows the number of lines and a gradation indicative data consists of triplets D0-D2 in drawing 2 .
[0046] Clock signal creatine kinase is inputted into a target one by one at a shift register SR, and a shift register SR derives on a target the memory control signals SR1 and SR2 for every source lines O1-ON shown at drawing 3 (3) - drawing 3 (6), respectively, --, SR (N-1) and SRN one by one based on this. The gradation indicative datas D0, D1, and D2 of the in-series triplet given from the display-control circuit 19 are inputted into a target one by one at the source driver 37, as shown to drawing 3 (2) by reference marks DA1, DA2, DA3, --, DAN corresponding to each source lines O1-ON. The gradation indicative datas D0-D3 inputted into the source driver 37 answer the memory control signals SR1-SRN, and a store is carried out one by one to a target at data memory DM.
[0047] The data latch circuit DL answers the latch signal LS outputted for every 1 horizontal scanning period WH shown in drawing 3 (7), corresponding to all the source lines O1-ON, carries out the store of each gradation indicative data of the parallel triplet by which the store is carried out to data memory DM, and latches it. The output of the data latch circuit DL is inputted into a comparator circuit CM. The output of a counter 44 is given to a comparator circuit CM. A counter 44 is reset by the latch signal LS given through a line 45, and carries out counting of the gradation clock signal CLK outputted from the gradation clock signal generating circuit 48.
[0048] In a comparator circuit CM, comparison with the output of the data latch circuit DL and the output of a counter 44 is performed, and if it agrees, a signal will be outputted to a switching circuit ASW. Reference voltage is supplied to the switching circuit ASW, and it is impressed by the source lines O1-ON through the end-connection children S1-SN. The voltage which a flow/interception of reference voltage are controlled by the output of a comparator circuit CM, and is impressed to the picture element electrode P is defined.
[0049] Above-mentioned operation is performed within 1 horizontal scanning period WH set by the horizontal synchronizing signal Hsyn shown in drawing 3 (1) created in the display-control circuit 39.
[0050] Drawing 4 is the circuit diagram showing the composition of the source 41 of reference voltage, and drawing 5 is the wave form chart of the reference voltage outputted from the source 41 of reference voltage. The reference supply circuit 41 divides and outputs from the voltage VAA more than grand voltage to the voltage VCC to eight stages with the gestalt of this operation for example.
[0051] The source 41 of reference voltage is constituted including the timing-control circuit 61, the voltage creation circuit 62, the voltage-selection circuit 63, the 1st inverter circuit 64, and the 2nd inverter circuit 65. The timing-control circuit 61 is constituted including flip-flops FF1-FF8. The latch signal LS which is the start pulse which clock signal creatine kinase is inputted into flip-flops FF1-FF8 in common, and is inputted into a flip-flop FF 1 is inputted into a target one by one for every start of clock signal creatine kinase at the flip-flop FF of the next step. The output of each flip-flop FF is given

to eight analog switches AS1-AS8 of the voltage-selection circuit 63, respectively, and controls opening and closing of the analog switch AS concerned. The output of the analog switches AS1-AS7 in the voltage-selection circuit 63 is connected in common.
[0052] In the source 41 of reference voltage, voltage VCC and voltage VAA are inputted into the 1st inverter circuit 64 and the 2nd inverter circuit 65, respectively. The 1st inverter circuit 64 is constituted by analog switches AS11 and AS12, and the output of the analog switch AS 12 of the voltage creation circuit 62 into which it is inputted into an edge on the other hand, and voltage VAA is inputted is inputted into the another side edge of the voltage creation circuit 62 for the output of the analog switch AS 11 into which voltage VCC is inputted. The inversion signal is inputted, respectively and, as for analog switches AS11 and AS12, opening and closing are controlled by the inversion signal.
[0053] The 2nd inverter circuit 65 is constituted by analog switches AS13 and AS14 and the inverter 66, and the output of the analog switch AS 14 of the voltage creation circuit 62 into which it is inputted into an edge on the other hand, and voltage VCC is inputted is inputted into the another side edge of the voltage creation circuit 62 for the output of the analog switch AS 13 into which voltage VAA is inputted. The signal which reversed the inversion signal by the inverter 66 is inputted into analog switches AS13 and AS14, and opening and closing of analog switches AS13 and AS14 are controlled by the output of this inverter 66. Therefore, one of the inverter circuits 64 and 65 will flow through the 1st inverter circuit 64 and the 2nd inverter circuit 65, and they give voltage VCC and voltage VAA by turns to the ends of the voltage creation circuit 62 by switching the high level and low level of a inversion signal.
[0054] The voltage creation circuit 62 is constituted from from voltage VCC before voltage VAA by the resistance R1-R7 connected to a serial, respectively. Resistance R1-R7 has the resistance defined beforehand. The voltage waveform corresponding to the gamma correction curve later mentioned by making the resistance of resistance R1-R7 into the value defined beforehand can be obtained.
[0055] The voltage of the one side edge of resistance R1 is inputted into the analog switch AS 1 of the voltage-selection circuit 63, and the voltage of the another side edge of resistance R7 is inputted into an analog switch AS 8. Each potential between resistance R1 - R7 is inputted into analog switches AS2-AS7.
[0056] Therefore, resistance R1-R7 divides into eight stages between two voltage inputted into the voltage creation circuit 62, and eight voltage is outputted to a target one by one according to the opening-and-closing timing of analog switches AS1-AS8 of inputting eight voltage, respectively.
[0057] Drawing 5 is drawing showing the voltage outputted from the source 41 of reference voltage. The wave shown in drawing 5 (1) shows the wave of the voltage used in the 3rd above-mentioned advanced technology, and is increasing linearly from the voltage VOFF of the off-level of liquid crystal the 1st order to the voltage VON of on-level in the period T1. The output of a period T1 is performed repeatedly.
[0058] The wave shown in drawing 5 (2) shows the voltage outputted from the source 41 of reference voltage, and the voltage of eight level from voltage VAA to voltage VCC is gradually outputted for every predetermined period which divided the period T2 equally. The aforementioned predetermined period is set based on the gradation clock CLK mentioned later. The level of six voltage between voltage VAA and voltage VCC is defined with the resistance of the aforementioned resistance R1-R7. Since a voltage level can be set up for every voltage, the voltage waveform approximated to the gamma correction curve shown with a dashed line in drawing 5 (2) can be outputted.
[0059] Drawing 6 is a wave form chart for explaining timing operation by the display-control circuit 39. The horizontal synchronizing signal Hsyn shown in drawing 6 (2) is generated respectively corresponding to the gate lines L1-LM for each [of the vertical synchronizing signal Vsyn shown in drawing 6 (1)] period of every. In drawing 6 (2), reference marks 1H and 2H, --, MH show the horizontal scanning period WH individually. During [each / WH] the horizontal scanning, in the gross, as DA11, DA12, --, the gradation indicative datas DA1-DAN shown by DA1M corresponding to the source lines O1-ON are shown in drawing 6 (3), it is generated from the display-control circuit 39, and is given to the source driver 17. In the signal shown in drawing 6 (3), since gradation indicative-data DA

given to a total of M source lines O1-ON is expressed collectively, the slash is given. Drawing 6 (4) shows the wave of the latch signal LS generated for every 1 horizontal scanning period WH.
[0060] The signal WHD shown in drawing 6 (5) shows the voltage level given to the source lines O1-ON in the gross according to the digital gradation indicative datas D0-D2 given in 1 horizontal scanning period WH. In the signal shown in drawing 6 (5), since the voltage level of a total of M source lines O1-ON is expressed collectively, the slash is given. One screen of a display panel 36 is expressed as a non-interlaced method in 1 vertical-scanning period. In the case of an interlace method, this invention can be carried out similarly.
[0061] Drawing 6 (6) - drawing 6 (8) show the wave of the gate signals G1, G2, and GM given to the gate lines L1, L2, and LM from a gate driver 18, respectively, respectively. For example, according to the j-th gate signal Gj being high-level, all (j, i) (j=1-M, i=1-N) of a total of N TFT T by which the gate electrode is connected to the gate line Lj are turned on, and the picture element electrode P (j, i) is charged according to the driver voltage given to the source line Oi at this time. One screen in 1 non-interlaced vertical-scanning period will be displayed by repeating above-mentioned operation a total of M times to each gate lines L1-LM. The polarity of the voltage given for every picture element electrodes of these is reversed for every field by the so-called alternating current driving method according to every 1 vertical-scanning period, and degradation of liquid crystal is suppressed by this.
[0062] Drawing 7 is the block diagram showing the concrete composition for every source line Oi of the source driver 37. When the gradation indicative data which consists of the in-series triplets D0-D2 is given to the memory control signal SRi from a shift register SR, the store of the data memory DMi which corresponds to the i-th source line (i=1-N) Oi individually is sampled and carried out. When the gradation indicative data of the parallel triplet by which the store is carried out to the individual data memory DMi is given to the latch signal LS, the store of the data latch circuit DLi which corresponds to the source line Oi of the data latch circuit DL individually is carried out, and it is latched. The gradation status signal of this parallel triplet is given to one input of the comparator circuit CMi which corresponds to each source line Oi of a comparator circuit CM individually through a line 43.
[0063] A counter 44 is formed in the source driver 37 again. This counter 44 answers the latch signal LS through a line 45, is reset, is initialized, and adds and carries out counting of the gradation clock signal CLK an enumerated data is made into zero and minds a line 46 after that. The output of the triplet showing this enumerated data is given to the input of another side of each comparator circuits CM1-CMN common to the source line Oi through a line 47. With the gestalt of this operation, the number of bits or the number of lines was set to n= 3.
[0064] The gradation clock signal CLK given to a counter 44 is drawn as an output of the gradation clock signal generating circuit 48 which carries out dividing of the above-mentioned clock signal creatine kinase.
[0065] Among Lines 42a and 42b and each source lines O1-ON to which the reference voltage from a voltage source 41 is given, the analog switch ASW1 which is a switching element for voltage impression - ASWN intervene individually in a switching circuit ASW. These analog switches ASW1 - ASWN constitute a switching circuit ASW.
[0066] Supposing the number of the reference marks N which show the number of the source line O is even, analog switch ASW1 and ASW3, --, line to which it connects with ASWN-1 and 2nd reference voltage is supplied 42b will be connected to analog switches ASW2 and ASW4, --, ASWN for line 42a to which the 1st reference voltage is supplied. The sense which carries out the change of potential, respectively differs, and the 1st and 2nd reference voltages take a contrastive voltage value on the basis of the opposite voltage VCOM impressed to a counterelectrode. In addition, the sense which carries out the change of potential for every frame is changed, and the 1st and 2nd reference voltages are set to be able to drive liquid crystal in alternating current. Moreover, in the source driver 37 shown in drawing 7 , although it has the composition that the gradation clock signal CLK is supplied from the exterior, the number of the signal input terminals prepared in the source driver 37 can be reduced by one by considering as the composition which forms the gradation clock signal generating circuit 48 in the source driver 37 as shown in drawing 2 .

[0067] Drawing 8 is a wave form chart for explaining operation of the source driver 37. When the gate signal Gj (j=1-M) which has the wave shown in drawing 8 (1) is given to a certain gate line Lj, the transistor T by which the gate electrode is connected to the gate line Lj flows during [WH] the horizontal scanning from the time t0 when the gate signal Gj is high-level to time t2, and the voltage of the source lines O1-ON is given to the picture element electrode P through the transistor T which has flowed. Moreover, gate signal Gj+1 shown in drawing 8 (2) in the horizontal scanning period from time t2 to time t4 is high-level.
[0068] The latch signal LS shown in drawing 8 (3) is generated synchronizing with the horizontal synchronizing signal Hsyn shown in drawing 3 (1). A counter 44 is initialized and reset while a gradation indicative data is latched to the data latch circuits DL1-DLN by this latch signal LS. The display-control circuit 39 gives a synchronizing signal through a line 49 (refer to drawing 1), and the source 41 of reference voltage derives the 1st reference voltage which increases gradually with the time progress shown in drawing 8 (4) to line 42a by this after time t0. In addition, although not illustrated in this timing chart, as for the 2nd reference voltage, elevation and descent change to the reverse sense with an equal voltage difference to the 1st reference voltage on the basis of for example, the opposite voltage VCOM below voltage VAA.
[0069] The gradation clock signal generating means 48 derives on a target the gradation clock signal CLK of two or more numbers more than the number of gradation which answers clock signal creatine kinase, therefore is expressed by the gradation indicative data during 1 horizontal scanning period WH synchronizing with a horizontal synchronizing signal Hsyn one by one time. In the gestalt of this operation, eight gradation clock signals CLK are generated in the horizontal scanning period WH noting that 8 gradation displays are performed from a gradation indicative data consisting of D0-D2 as data of a triplet as shown in drawing 8 (5) for example. In addition, the number of the gradation clock signals CLK which make it generate in the aforementioned horizontal scanning period WH may be a value exceeding 8.
[0070] Counting of this gradation clock signal CLK is carried out by the counter 44, and it is given as mentioned above to the input of another side of a comparator circuit CMi through a line 47, respectively. The enumerated data of a counter 44 is shown by reference marks 1, 2, 3, --, 8 in drawing 8 (5).
[0071] For example, when the gradation indicative data latched to the latch circuit DLi is "2", the output of a comparator circuit CMi shown in drawing 8 (6) becomes high-level at time t0-t1. The aforementioned output showing a gradation indicative data "2" is given to one input 43 of a comparator circuit CMi, and the enumerated data of a counter 44 is given to the input of another side as mentioned above. The output wave of a comparator circuit CMi shown in drawing 8 (6) is given to an analog switch ASWi as a switching control signal.
[0072] It supposes that this switching control signal is high-level when the enumerated data of the counter 44 which performs addition operation is under a value corresponding to a gradation indicative data "2", and it has flowed through an analog switch ASWi, and the enumerated data of the counter 44 serves as a low level at the time t1 which became beyond the value corresponding to a gradation indicative data "2", and intercepts an analog switch ASWi. In this way, the driver voltage which has the wave shown in drawing 8 (7) is impressed to the source line Oi from the end-connection child Si. At time t0-t1, the reference voltage wave shown in drawing 8 (4) is given to the source line Oi as it is.
[0073] Henceforth [time t1], since an analog switch ASWi is intercepted as mentioned above, it becomes [that the driver voltage V2 corresponding to a gradation indicative data "2" is given to the picture element electrode P with as, and], a charge is accumulated by part for the picture element display of a display panel, and voltage V2 is held. Moreover, the wavy line shows the opposite voltage VCOM impressed to a counterelectrode to drawing 8 (7). The opposite voltage VCOM is fixed in time t0-t4.
[0074] When the gradation indicative data which is latched to a latch circuit DLi and drawn from time t2 in the horizontal scanning period by time t4 is "6", a comparator circuit CMi gives the signal which is high level until the enumerated data of a counter 44 is in agreement with an analog switch ASWi at a gradation indicative data "6." An analog switch ASWi is intercepted at the time t3 whose

aforementioned enumerated data corresponds with a gradation indicative data. That is, in time t2-t3, an analog switch ASWi is having flowed with as.
[0075] Since the analog switch ASWi has flowed at time t2-t3, driver voltage V6 is drawn from a line 42 by the source line Oi through an analog switch ASWi and the end-connection child Si. The voltage V6 corresponding to the gradation indicative data "6" is held through the transistor T which has flowed at the picture element electrode P.
[0076] Such operation is repeated for every gate lines L1-LM for every horizontal scanning period WH, and the driver voltage corresponding to the gradation indicative data of the picture element electrode P is held over 1 vertical-scanning period.
[0077] Drawing 9 is the representative circuit schematic having simplified and shown the liquid crystal display panel 36, in order to explain the principle of this invention. In this invention, the electrostatic capacity Cs which the source line Oi has considers the circuit which was connected in series and which, so to speak, has the function of a low pass filter to be the resistance Rs of one source line Oi set as the drive object of the source driver 37.
[0078] The equivalence-capacity which the picture element electrode P has is shown by the reference mark CL. The electrostatic capacity CL of this picture element electrode P is fully small compared with the capacity Cs of the source line Oi (Cs>>CL). Therefore, the voltage given to the picture element electrode P becomes the same value as Resistance Rs and the voltage of the node 51 with electrostatic capacity Cs. Therefore, reference voltage is given to the source line Oi through an analog switch ASWi, and the picture element electrode P is made to charge in the equal circuit shown in drawing 9 which has a function as this low pass filter. For example, when it is time constant Cs-Rs=10-7, the flow time of this analog switch ASWi should just be more than at least 20-30microsec.
[0079] Thus, the liquid crystal display panel 56 uses positively Resistance Rs and electrostatic capacity Cs of the source line Oi which it has unescapable, and makes voltage hold to the picture element electrode P in this invention. Between the gate lines L (j-1) and the source lines Oi which are previously scanned in time by only one scanning direction in other gestalten of operation of this invention rather than the gate line Lj to which the gate electrode of Transistor T is connected, moreover, auxiliary capacity You may make it increase substantially the capacity for being formed on a substrate and while the picture element electrode P being formed holding voltage to the picture element electrode P.
[0080] Drawing 10 is drawing for explaining operation of the source driver 137 which is the 2nd gestalt of operation of this invention. Since the source driver 137 is the same composition as the above-mentioned source driver 37, it omits the explanation about composition, and it explains it about the feature of the source driver 137 as compared with the source driver 37. Drawing 10 (1) Since each signal shown in - (3) and (5) is the same as that of drawing 8 (1) - (3) and (5) respectively, explanation is omitted.
[0081] Although the 1st reference voltage shown in drawing 8 (4) was gradually outputted from voltage VAA to voltage VDD for every horizontal scanning period, for every horizontal scanning period, the 1st reference voltage shown in drawing 10 (4) switches elevation from voltage VAA to voltage VDD, and the descent from voltage VDD to voltage VAA, and is outputted. Moreover, the 2nd reference voltage which is not illustrated turns into the 1st reference voltage with the voltage waveform shifted 1 horizontal scanning period every, respectively.
[0082] In case the source lines O1-ON are driven by the source driver 137, the opposite voltage VCOM shown with a dashed line by drawing 10 (7) is impressed to a counterelectrode. In the horizontal scanning period from time t5 to time t7, the opposite voltage VCOM turns into the grand voltage VGND, for example, and turns into the voltage VOC defined, for example more than voltage VCC in the horizontal scanning period from time t7 to time t9. In addition, it is determined that each voltage serves as VOC-VCC=VAA-VCOM.
[0083] In drawing 10 , the signal which is high level is given until the enumerated data of a counter 44 is in agreement with a gradation indicative data "4" as shown in an analog switch ASWi at drawing 10 (6), since the gradation indicative data which is latched to a latch circuit DLi and drawn is "4." By this, an analog switch ASWi is having flowed with as in time t5-t6. Therefore, it is given through an analog

switch ASWi and the end-connection child Si from a line 42, for example, the driver voltage V4 which has the wave the 1st reference voltage is indicated to be to the source line Oi at drawing 10 (7) is drawn, and the voltage V4 corresponding to the gradation indicative data "4" is held through the transistor T which has flowed at the picture element electrode P. Such operation is performed to each gate lines L1-LM for every horizontal scanning period WH, the driver voltage corresponding to the gradation indicative data of the picture element electrode P is impressed, and it is held over 1 vertical-scanning period.

[0084] Drawing 11 is the block diagram showing concretely the composition of a part of source driver 37a which is the 3rd gestalt of operation of this invention. Since the gestalt of implementation of this invention is similar to the gestalt of implementation of the above-mentioned invention, the same reference mark is given to a corresponding portion, and explanation is omitted. Although the source 41 of reference voltage is established in the exterior of the source driver 37 and it can cook with the gestalt of each operation shown in above-mentioned drawing 1 - drawing 10 With the gestalt of this operation Digital one / analog converters 52a and 52b (when naming generically) which are the composition respectively same in source driver 37a ("DAC" is called henceforth) And it uses ******** 52, an inverter 53 is built in and a single semiconductor integrated circuit realizes source driver 37a with a residual circuit element.

[0085] The signal showing the enumerated data drawn from the counter 44 mentioned above by the line 47 is given, respectively, and DACs 52a and 52b output the voltage which has a voltage value corresponding to the enumerated data. The output of DAC52a is supplied to an analog switch ASWi like the 1st above-mentioned reference voltage, and the output of DAC54b is supplied to an analog switch ASWi like the 2nd above-mentioned reference voltage. Other composition is the same as that of the gestalt of each above-mentioned operation. The output of DAC52a is shown in below-mentioned drawing 13 (6).

[0086] Drawing 12 is the circuit diagram showing the composition of DAC52. DAC52 is constituted including resistance R1-R8, inverters NG1-NG3, and switches SW1-SW14.

[0087] Resistance R is connected in series in an order from R1, the terminal by the side of resistance R1 is connected to voltage VCC, and the terminal by the side of resistance R8 is grounded. Between each resistance R and between resistance R8 and grand voltage, switches SW1-SW8 are prepared for a target one by one, respectively. Two switches SW are carried out to turn from a switch SW1 at a group, and the output of Switch SW is inputted into switches SW9-SW12, respectively. Furthermore, the output of switches SW9 and SW10 is inputted into a switch SW13, and the output of switches SW11 and SW12 is inputted into a switch SW14. The output of switches SW13 and SW14 is connected to an output terminal ST in common.

[0088] The output of a counter 44 is made into signals CO1, CO2, and CO3 from a lower bit at turn. Switches SW1, SW3, SW5, and SW7 flow with a signal CO 1, and switches SW2, SW4, SW6, and SW8 flow through a signal CO 1 with the signal reversed by the inverter NG 1. Moreover, switches SW9 and SW11 flow with a signal CO 2, and switches SW10 and SW12 flow through a signal CO 2 with the signal reversed by the inverter NG 2. Furthermore, a switch SW13 flows with a signal CO 3, and a switch SW14 flows through a signal CO 3 with the signal reversed by the inverter NG 3. The output from one switch of the switches SW13 and SW14 is given to an output terminal ST.

[0089] Drawing 13 is a wave form chart for explaining operation of source driver 37a shown in drawing 11 . The transistor T by which the gate signal Gj shown in a certain gate line Lj at drawing 13 (1) is drawn, and the gate electrode is connected to the gate line Lj flows, and it is generated as the latch signal LS is shown in drawing 13 (3) for every horizontal scanning period at this time. Gate signal Gj+1 impressed to gate line Lj+1 is shown in drawing 13 (2). The gradation clock signal shown in drawing 13 (4) is generated at a line 46, and it is given to a counter 44. Such each wave of drawing 13 (1) - drawing 13 (4) is the same as each wave of above-mentioned drawing 8 (1) - drawing 8 (3), and drawing 8 (5) respectively.

[0090] A counter 44 is especially given to DAC52 with the gestalt of this operation while it draws the signal which consists of n bits showing the enumerated data shown in drawing 13 (5) on a line 47 and

gives it to it common to comparator circuits CM1-CMN.
[0091] DAC52 answers the signal showing the enumerated data through a line 47, and outputs the voltage which rises gradually and changes with the time progress shown in drawing 13 (5). It follows, for example, when a gradation indicative data is "2" like the above-mentioned, only the period of time t10-t11 draws a high-level signal, and a comparator circuit CMi makes it flow through an analog switch ASWi, as shown in drawing 13 (7). When an analog switch ASWi flows, it is drawn and the driver voltage corresponding to a gradation indicative data "2" is impressed [at the source line Oi] to the corresponding picture element electrode P drawing 13 (8) so that it may be shown. The aforementioned driver voltage is held till the time t12 which a horizontal scanning period ends.
[0092] Moreover, since a comparator circuit CMi derives a signal high-level till the time t13 whose enumerated data of a counter 44 corresponds with a gradation indicative data "6" from time t12 when the gradation indicative data in the horizontal scanning period from time t12 to time t14 is "6", the driver voltage corresponding to a gradation indicative data "6" is drawn by the source line Oi through an analog switch ASWi. The driver voltage impressed to the picture element electrode P in time t13 is held till time t14.
[0093] As mentioned above, according to the 3rd gestalt of operation of this invention, the number of end-connection children for not supplying reference voltage from the external source 41 (referring to drawing 1) of reference voltage, and supplying reference voltage in source driver 37a realized by the semiconductor integrated circuit, by building in a counter 44, and the digital one/analog converter 52, and creating the reference voltage for a gradation display, can be reduced, and simplification of composition can be attained. Other composition is the same as that of the gestalt of implementation of the above-mentioned invention.
[0094] Drawing 14 is the block diagram showing the composition of a part of source driver 37b which is the 4th gestalt of operation of this invention. Since the gestalt of this operation is also similar to the gestalt of each above-mentioned operation, the same reference mark is given to a corresponding portion, and explanation is omitted.
[0095] With the gestalt of this operation, it transposes to the latch circuit DLi in the gestalt of each above-mentioned operation, and the value DEi which the enumerated data of the backward counter CNTi defines beforehand further, for example, the detection decoder which detects having become zero with the gestalt of this operation, is established using backward counter CNTi. Other composition is the same as that of the gestalt of each above-mentioned operation, and the 1st and 2nd reference voltages to which it follows on time progress, and voltage rises or descends gradually are further drawn from a line 42 by each source line Oi through the end-connection child Si through each analog switch ASWi.
[0096] Drawing 15 is the block diagram showing the concrete composition of backward counter CNTi and the detection decoder DEi. In drawing 15 , although the example by which the gradation indicative data is constituted from 6 bits is shown, you may be the arbitrary numbers of bits.
[0097] The gradation indicative datas D0-D5 of 6 bits of parallel from the data memory circuit DMi are given to set input terminal S* (* means reversal) of the D form flip-flops F0-F5 with RS (reset, set) through NAND gates NG0-NG5 by which the latch signal is supplied to one input terminal. Moreover, the gradation indicative datas D0-D5 inputted into inverter circuits N0-N5 are inputted into reset input terminal R* through NAND gates NG00-NG05 by which the latch signal is supplied to one input terminal, respectively.
[0098] the aforementioned flip-flops F0-F5 -- a serial -- or cascade connection is carried out The latch signal LS which minds [of NAND gates NG0-NG5 and another side of NG00-NG05] a line 45 is inputted, respectively. Output Q* of flip-flops F0-F5 is given to the data input terminal D, respectively.
[0099] The output of NAND gate NGI0 is given to the clocked-into terminal creatine kinase of the flip-flop F0 of the first rank. The gradation clock signal CLK which minds [of NAND gate NGI0 / one] a line 46 is inputted, an inverter circuit NI0 is reversed and the output of the NOR gate 54 mentioned later is given to the input of another side. The output Q of the flip-flops F0-F4 of one step ago is given to the clocked-into terminal creatine kinase of flip-flops F1-F5, respectively.
[0100] Operation of backward counter CNTi is explained. When the latch signal LS is inputted into

backward counter CNTi, each bit of the gradation indicative datas D0-D5 is loaded to flip-flops F0-F5. The gradation indicative data loaded to flip-flops F0-F5 answers a gradation clock signal, and is subtracted by the target one by one. If all the outputs Q of the flip-flops F0-F5 which constitute backward counter CNTi become logic "0", this will be detected in the detection decoder DEi.
[0101] The detection decoder DEi contains the NOR gate 54 and an inverter circuit NI1. The output Q of flip-flops F0-F5 is given to the NOR gate 54. The output of the NOR gate 54 is given to an inverter circuit NI1 while it is given to the inverter circuit NI0 with which the above-mentioned backward counter CNTi is equipped.
[0102] The output of an inverter circuit NI1 is given to an analog switch ASWi, and when the output of an inverter circuit NI1 is high-level, an analog switch ASWi flows. When an analog switch ASWi flows, it is impressed by the source line Oi which corresponds through the end-connection child Si, and the reference voltage currently supplied to the line 42 is given to the picture element electrode P, and is held.
[0103] The output Q of the flip-flops F0-F5 contained in backward counter CNTi of the output of the NOR gate 54 is a low level when at least 1 bit is logic "1." Therefore, the output of an inverter circuit NI1 becomes high-level, and the analog switch ASWi is having flowed with as.
[0104] If all the outputs Q of flip-flops F0-F5 become logic "0", the output of the NOR gate 54 becomes high-level, the output of an inverter circuit NI1 serves as a low level according to this, and the impedance which intercepted the analog switch ASWi and looked at source driver 37b from the output terminal Si will be in a high impedance state.
[0105] Simultaneously with this, the output of the logic "1" of the NOR gate 54 is given to NAND gate NG10 through an inverter circuit NI0, and the gradation clock signal CLK ceases to be given to the flip-flop F0 of the first rank. in this way, subtraction of backward counter CNTi -- counting -- operation stops, and again, this state is maintained until the latch signal LS is inputted
[0106] The same wave form chart as drawing 8 is obtained, and operation is performed [in / the gestalt of each aforementioned implementation / as mentioned above]. Therefore, when the enumerated data of backward counter CNTi exceeds zero (i.e., when an enumerated data becomes zero with the gestalt of this operation) (i.e., when it carries out to having made it freely flow through an analog switch ASWi and an enumerated data becomes below zero until the enumerated data was set to 1), an analog switch ASWi is intercepted.
[0107] Drawing 16 is the block diagram showing the composition of a part of source driver 37c which is the 5th gestalt of operation of this invention. Since the gestalt of this operation is also similar to the gestalt of the above-mentioned operation, the same reference mark is given to a corresponding portion, and explanation is omitted.
[0108] Opening and closing of an analog switch ASWi are controlled by the gestalt of this operation using backward counter CNTi and the detection decoder DEi like the 4th gestalt of the above-mentioned operation. The feature of the gestalt of this operation is creating reference voltage inside source driver 37c like the 3rd gestalt of the above-mentioned operation by forming a counter 44, DACs 52a and 52b, and an inverter 53 in source driver 37c.
[0109] In source driver 37c, a counter 44 supplies an output to DAC52a and DAC52b. Each output of DAC52 is given to the analog switch ASWi which corresponds, respectively.
[0110] Since the reference voltage for performing a gradation display is created within source driver 37c as mentioned above according to the 5th gestalt of operation of this invention, the terminal into which the reference voltage from the source 41 of reference voltage shown, for example in drawing 1 is inputted is unnecessary, the number of input terminals can be reduced and simplification of composition can be attained. About other composition, it is the same as that of the gestalt of each above-mentioned operation.
[0111] With the gestalt of implementation of above-mentioned invention, the source 41 of reference voltage, and the digital one/analog converter 52 may be the composition that this reference voltage descends with time progress as other gestalten of operation of this invention although it constitutes to generate the reference voltage which rises with time progress, and the ANAROKU switch ASWi is

considered as the composition through which only time to answer the output of a comparator circuit CMi and the detection decoder DEi, and set beforehand flows at this time. It is set to sufficient time for calling it this time setting beforehand to be able to impress voltage to the picture element electrode P, and able to hold it.

[0112] In addition, although the gestalt of each operation mentioned above mainly explained the case where eight gradation was displayed, using the data of a triplet as a gradation indicative data, much more numbers of gradation can be displayed by preparing the reference voltage of the number corresponding to the data of more numbers of bits, and the data concerned.

[0113]

[Effect of the Invention] According to this invention, the periodic voltage which rises or descends with time progress is generated as mentioned above. Since the aforementioned voltage at the time of the time of the time corresponding to the gradation indicative data passing for every period of that or the aforementioned voltage becoming a voltage value corresponding to a gradation indicative data is impressed to electrodes, such as a picture element electrode of a display panel, and it was made to make it hold A driving gear is good with one terminal into which it is not necessary to prepare the terminal for two or more voltage inputs, and the aforementioned voltage is inputted. Moreover, switching elements for voltage impression, such as an analog switch, can reduce the number of end-connection children, the number of analog switches, etc. that single one piece should just be prepared corresponding to lines, such as a source line, performing a multi-gradation display. By this, since the miniaturization of semiconductor chips, such as a source driver, low-power-izing, low-cost-izing, high-density-assembly-ization, etc. are attained, mass-production-ization of semiconductor integrated circuits, such as a source driver which displays many gradation, is attained easily.

[0114] Moreover, according to this invention, the outstanding effect that the picture element electrode of a large number which intervene dielectric layers, such as liquid crystal, can carry out this invention to the substrate of another side which while was prepared and counters a substrate, using the ordinary display panel in which the single common electrode common to the picture element electrode of aforementioned a large number was formed, for example as it is, and this invention can carry out easily in relation to the existing display panel by this is also attained.

[0115] Furthermore, according to this invention, it is not necessary to form the capacitor for sample hold described in relation to above-mentioned drawing 20 out of a display panel and, complicated circuits, such as an operational amplifier, are not needed, the miniaturization of composition can be attained by this, and especially this is set to one of the important effects of this invention, when a semiconductor integrated circuit realizes this invention.

[0116] Furthermore, according to this invention, by simplifying composition as mentioned above, dispersion in the property of a circuit element is suppressed and the outstanding effect that display grace can be improved by this is also attained.

[0117] Furthermore, according to this invention, for example for every period, such as 1 horizontal scanning period, by the number more than the number of gradation which should indicate by gradation Generate the gradation clock signal which is a period shorter than the aforementioned period from a gradation clock signal generating means, and counting is added and carried out by the counter. Since the switching element for voltage impression is turned on or OFF controlled when the enumerated data turns into a value corresponding to a gradation indicative data The same gradation display as usual can be performed being able to impress the voltage corresponding to a gradation indicative data to the electrode of a display panel certainly, and attaining simplification of composition, such as curtailment of the terminal for a voltage input, and curtailment of the number for voltage impression of switching elements.

[0118] Furthermore, according to this invention, for every period, such as 1 horizontal scanning period, set the value corresponding to the gradation indicative data as a backward counter, and it subtracts for whenever [of reception of a gradation clock signal / every]. Since it is made to control a flow/interception of the switching element for voltage impression when the subtracted enumerated data turns into the value defined beforehand, for example, zero The voltage corresponding to the gradation

indicative data can be certainly impressed to the electrode of a display panel, and simplification of composition can be attained by this as well as ****.

[0119] The voltage source which furthermore generates the voltage which rises or descends with time progress according to this invention Based on the enumerated data of the counter which carries out counting of the gradation clock signal from a gradation clock signal generating means, and outputs it, generate voltage, for example, since it is realizable with digital one/analog converter The voltage which synchronizes correctly and changes to a gradation clock signal gradually can be obtained easily, and the voltage corresponding to the gradation indicative data can be impressed to the electrode of a display panel to exact timing.

[0120] Realizing is possible, without furthermore, preparing separately the capacitor which tends to turn maintenance of the voltage corresponding to a gradation indicative data on a large scale according to this invention, since it was made to perform a gradation display drive using charge/electric discharge of the charge of electrodes, such as an active-matrix display panel or a simple matrix display panel, using diclectric layers, such as liquid crystal or electroluminescence material.

[Translation done.]

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【図９】液晶表示パネル３６に電圧が保持される原理を説明するための等価回路図である。
【図１０】本発明の実施の第２の形態であるソースドライバ１３７の動作を説明するための波形図である。
【図１１】本発明の実施の第３の形態であるソースドライバ３７ａの具体的な構成を示すブロック図である。
【図１２】デジタルアナログコンバータ５２ａ，５２ｂの回路図である。
【図１３】ソースドライバ３７ａの動作を説明するための波形図である。
【図１４】本発明の実施の第４の形態であるソースドライバ３７ｂの具体的な構成を示すブロック図である。
【図１５】図１４に示される実施の形態における減算カウンタＣＮＴｉと検出デコーダＤＥｉの具体的な構成を示すブロック図である。
【図１６】本発明の実施の第５の形態であるソースドライバ３７ｃの具体的な構成を示すブロック図である。
【図１７】第１の先行技術の全体の構成を簡略化して示すブロック図である。
【図１８】図１７に示されるソースドライバ１２の一部の構成を具体的に示すブロック図である。
【図１９】第２の先行技術の全体の構成を簡略化して示すブロック図である。
【図２０】第３の先行技術の構成を簡略化して示すブロック図である。
【図２１】第４の先行技術の構成を簡略化して示すブロック図である。
【図２２】図２１に示されるＸドライバ１２０の動作を説明するための波形図である。

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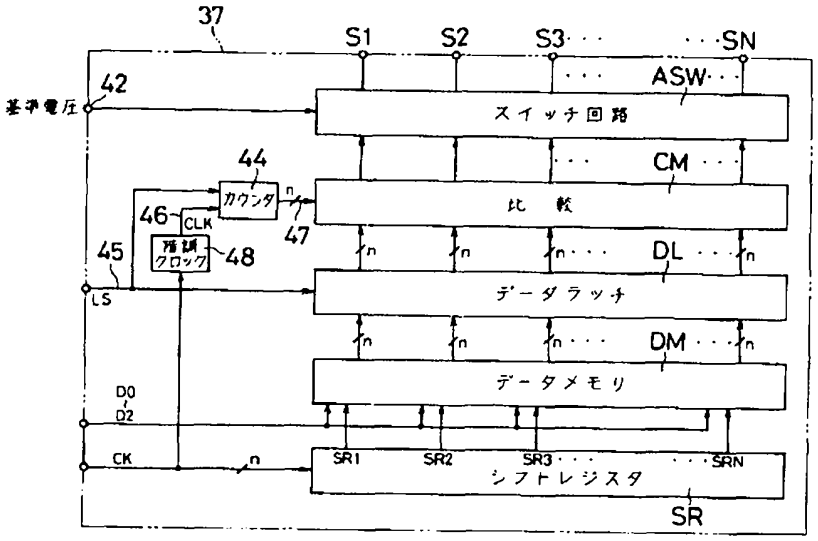
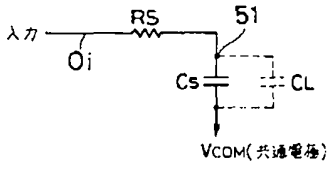
【符号の説明】
３６　アクティブマトリクス形液晶表示パネル
３７，３７ａ，３７ｂ，３７ｃ，１３７　ソースドライバ
３８　ゲートドライバ
３９　表示制御回路
４１　基準電圧源
４４　カウンタ
４８　階調クロック信号発生手段
５２　デジタル／アナログコンバータ
５４　ＮＯＲゲート
ＡＳＷ１～ＡＳＷＮ　アナログスイッチ
ＣＫ　クロック信号
ＣＬＫ　階調クロック信号
ＣＭ　比較回路
ＣＮＴｉ　減算カウンタ
Ｄ０～Ｄ２　階調表示データ
ＤＥｉ　検出デコーダ
ＤＬ　データラッチ回路
ＤＭ　データメモリ
Ｆ０～Ｆ５　フリップフロップ
Ｌ１～ＬＭ　ゲートライン
ＬＳ　ラッチ信号
Ｏ１～ＯＮ　ソースライン
Ｐ　絵素電極
Ｓ１～ＳＮ，Ｇ１～ＧＭ　接続端子
ＳＲ　シフトレジスタ
Ｔ　薄膜トランジスタ
ＷＨ　１水平走査期間

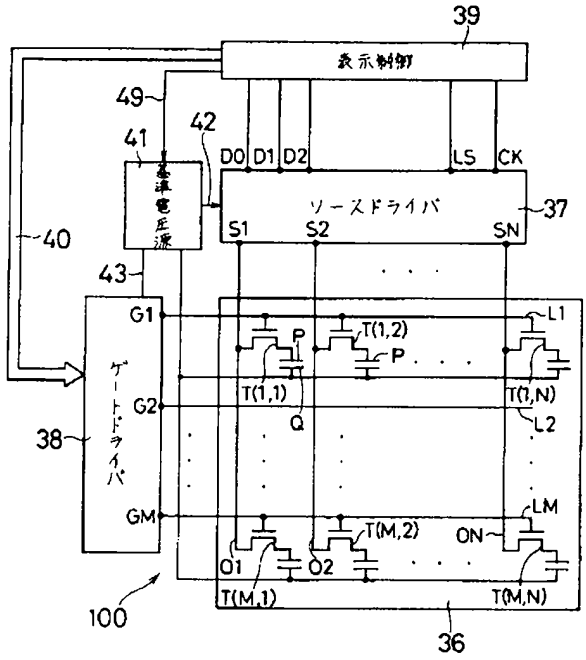
【図２】



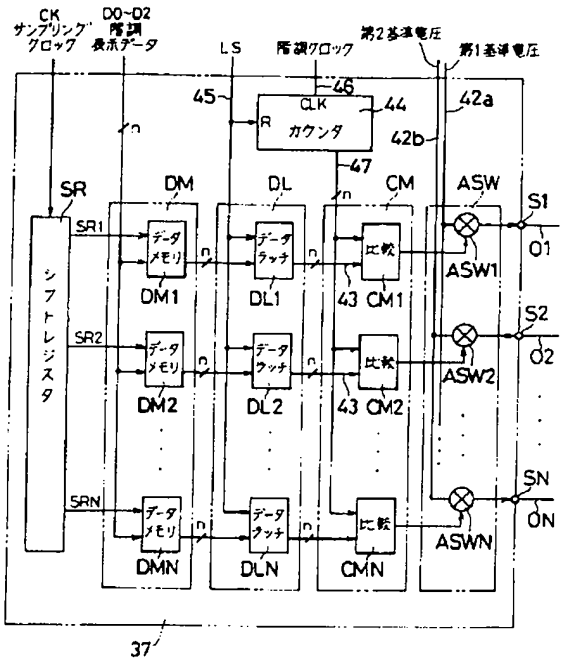
【図９】



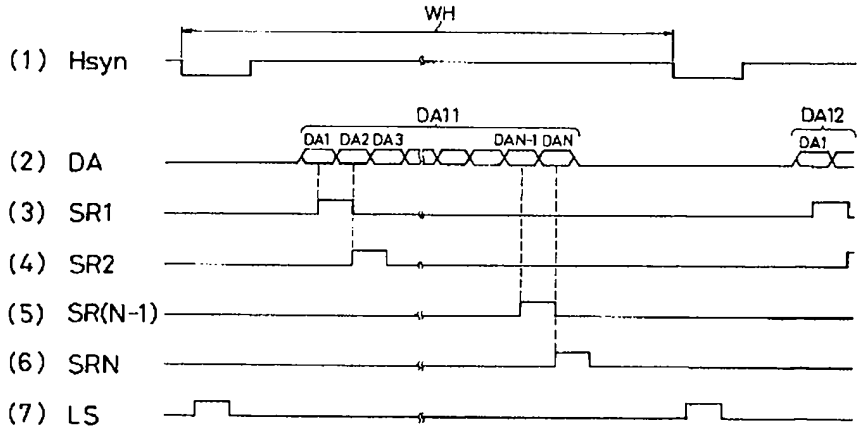
【図1】


39
表示制御
49
41
42
D0 D1 D2
LS CK
基準電圧源
ソースドライバ
37
40
S1 S2 SN
43
G1
L1
P
T(1,2)
T(1,1)
T(1,N)
Q
G2
L2
38
ゲートドライバ
GM
LM
ON
T(M,2)
O1 O2
T(M,1)
T(M,N)
100
36

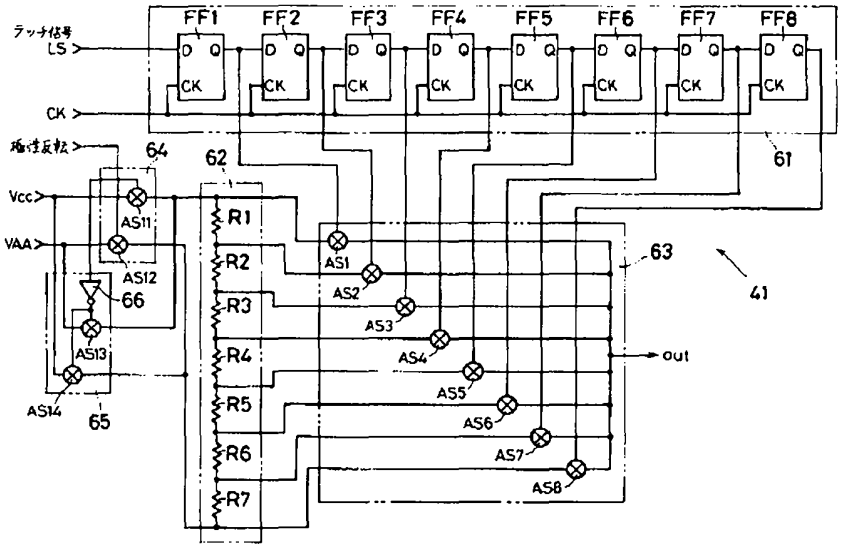
【図7】


CK
サンプリングクロック
D0~D2
階調表示データ
LS
階調クロック
第2基準電圧
第1基準電圧
45
46
CLK
カウンタ
44
42a
42b
47
SR
DM
DL
CM
ASW
S1
シフトレジスタ
SR1
データメモリ
データラッチ
比較
ASW1
O1
DM1
DL1
43
CM1
SR2
S2
ASW2
O2
DM2
DL2
CM2
SRN
SN
ON
DMN
DLN
CMN
ASWN
37

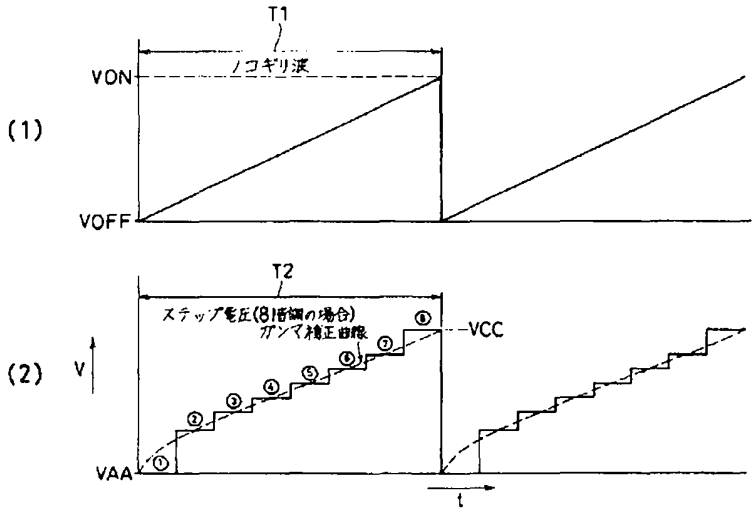
【図3】


WH
(1) Hsyn
DA11
DA1 DA2 DA3
DAN-1 DAN
DA12
DA1
(2) DA
(3) SR1
(4) SR2
(5) SR(N-1)
(6) SRN
(7) LS

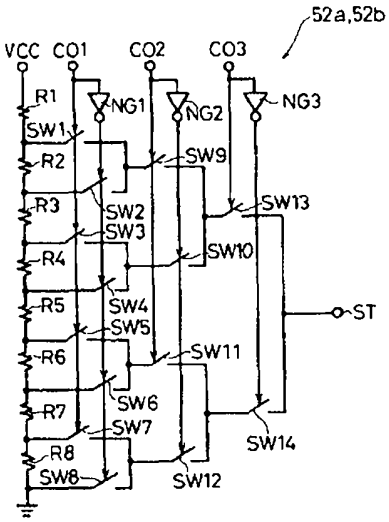
【図4】


FF1
FF2
FF3
FF4
FF5
FF6
FF7
FF8
D
Q
CK
LS
CK
Vcc
VAA
64
62
61
63
41
AS11
AS12
AS13
AS14
AS1
AS2
AS3
AS4
AS5
AS6
AS7
AS8
66
65
R1
R2
R3
R4
R5
R6
R7
out

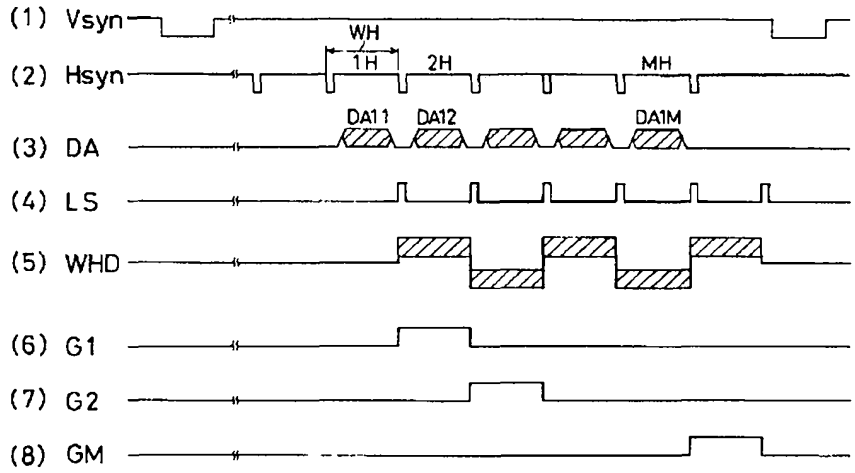
【図5】


T1
VON
ノコギリ波
VOFF
(1)
T2
ステップ電圧(8bit階調の場合)
ガンマ補正曲線
VCC
(2)
V
VAA
t

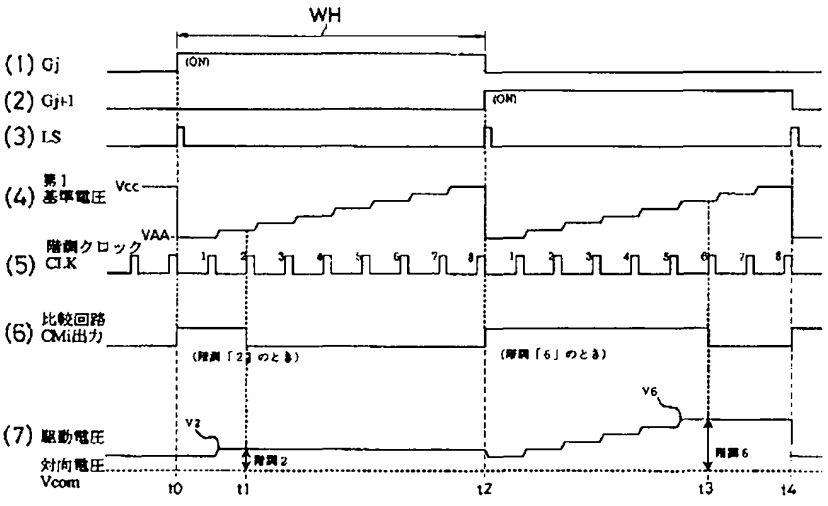
【図12】


52a,52b
VCC
CO1
CO2
CO3
R1
R2
R3
R4
R5
R6
R7
R8
NG1
NG2
NG3
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW13
SW14
ST

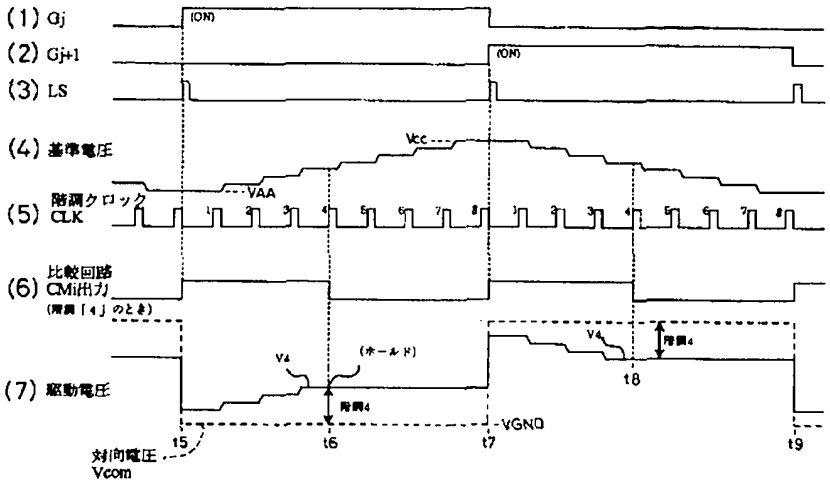
【図6】


(1) Vsyn
WH
1H
2H
MH
(2) Hsyn
DA11
DA12
DA1M
(3) DA
(4) LS
(5) WHD
(6) G1
(7) G2
(8) GM

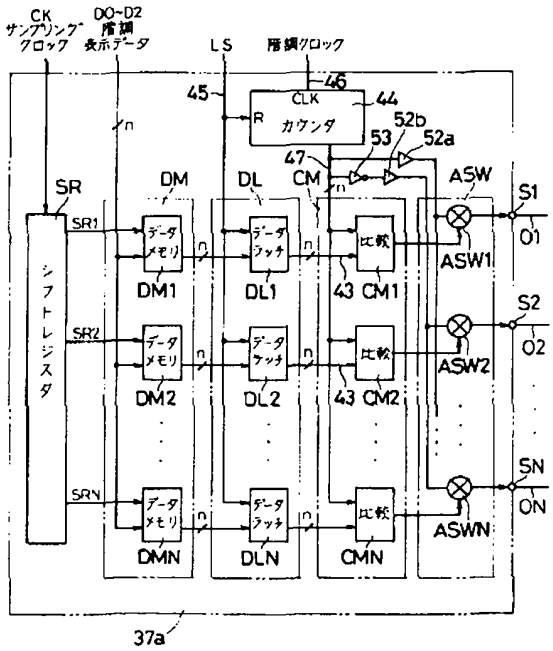
【図8】


WH
(1) Gj
(ON)
(2) Gj+1
(ON)
(3) LS
(4) 第1基準電圧
Vcc
VAA
(5) 階調クロック CLK
(6) 比較回路 CMi出力
(階調「2」のとき)
(階調「6」のとき)
V6
V2
(7) 駆動電圧
階調2
階調6
対向電圧 Vcom
t0
t1
t2
t3
t4

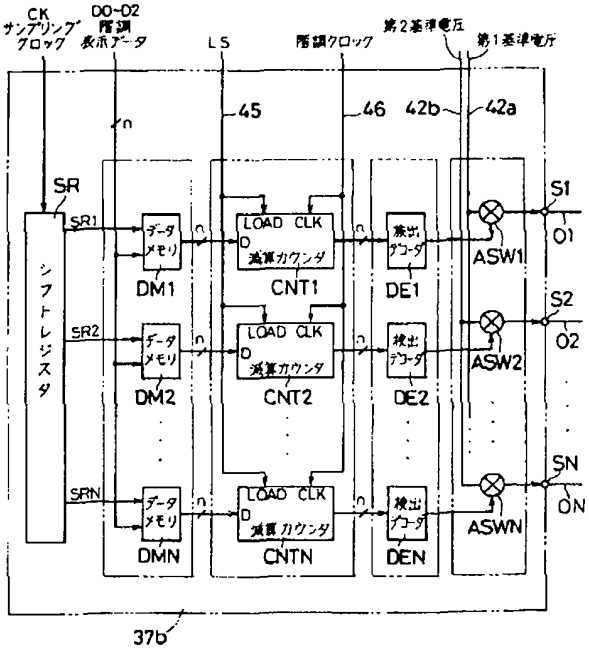
【図10】


(1) Gj
(2) Gj+1
(3) LS
(4) 基準電圧
(5) 階調クロック CLK
(6) 比較回路 CMi出力 (階調「4」のとき)
(7) 駆動電圧
(ON)
Vcc
VAA
V4
(ホールド)
階調4
VGND
対向電圧 Vcom
t5
t6
t7
t8
t9

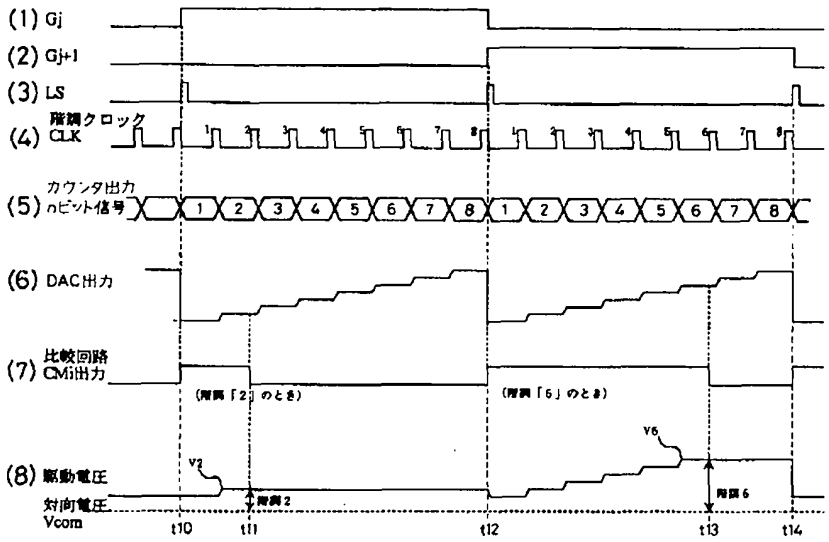
【図11】


CK
サンプリング クロック
D0~D2
階調 表示データ
LS
階調クロック
45
46
CLK
R
カウンタ
44
52b
53
52a
47
SR
DM
DL
CM
ASW
S1
O1
SR1
データ メモリ
DM1
データ ラッチ
DL1
比較
43 CM1
ASW1
S2
O2
SR2
DM2
DL2
43 CM2
ASW2
SRN
DMN
DLN
CMN
ASWN
SN
ON
シフトレジスタ
n
37a

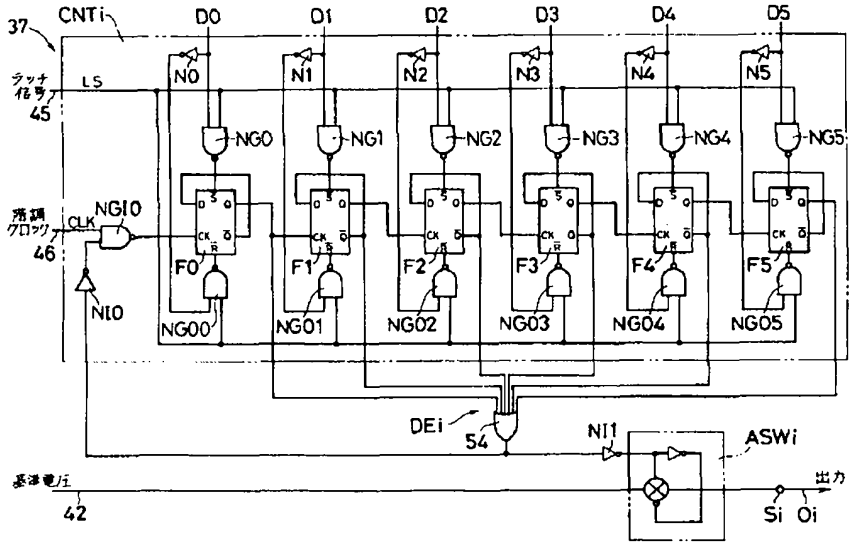
【図14】


CK
サンプリング クロック
D0~D2
階調 表示データ
LS
階調クロック
第2基準電圧
第1基準電圧
45
46
42b
42a
SR
SR1
データ メモリ
DM1
LOAD CLK
D
減算カウンタ
CNT1
検出 デコーダ
DE1
ASW1
S1
O1
SR2
DM2
CNT2
DE2
ASW2
S2
O2
SRN
DMN
CNTN
DEN
ASWN
SN
ON
シフトレジスタ
n
37b

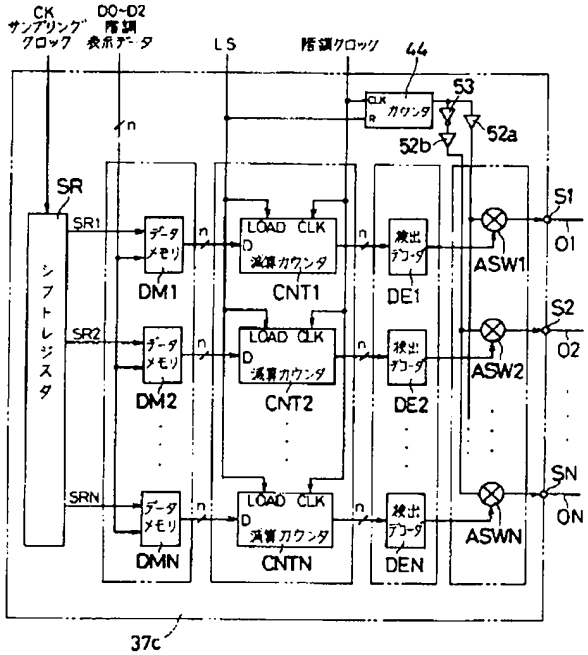
【図13】


(1) Gj
(2) Gj+1
(3) LS
(4) 階調クロック CLK
(5) カウンタ出力 nビット信号
(6) DAC出力
(7) 比較回路 CMi出力
(階調「2」のとき)
(階調「6」のとき)
(8) 駆動電圧
対向電圧 Vcom
V2
V6
階調2
階調6
t10
t11
t12
t13
t14

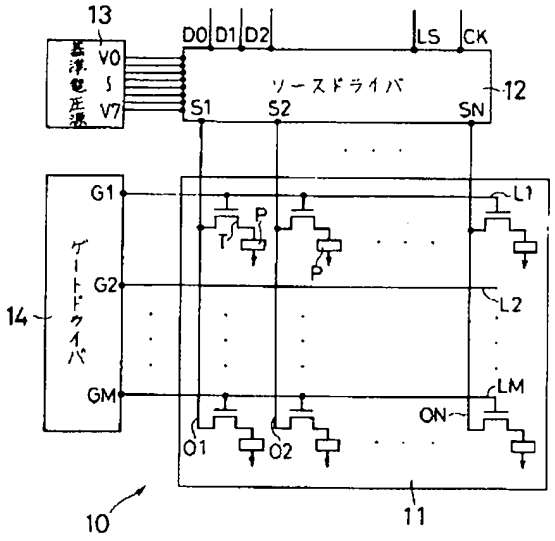
【図15】


37
CNTi
D0
D1
D2
D3
D4
D5
ラッチ信号
45
LS
N0
N1
N2
N3
N4
N5
NG0
NG1
NG2
NG3
NG4
NG5
階調クロック
46
CLK
NGI0
NI0
F0
F1
F2
F3
F4
F5
NG00
NG01
NG02
NG03
NG04
NG05
DEi
54
NI1
ASWi
基準電圧
42
出力
Si
Oi

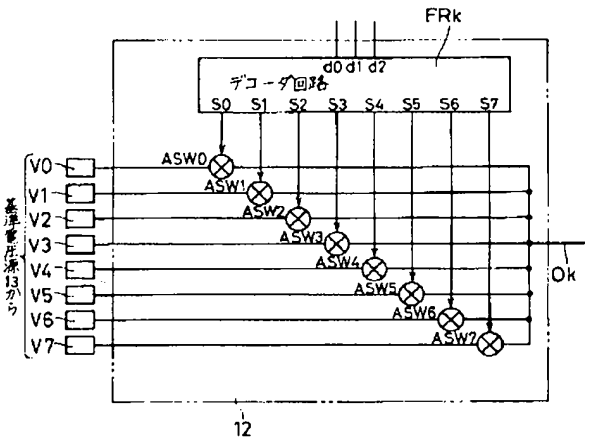
【図１６】



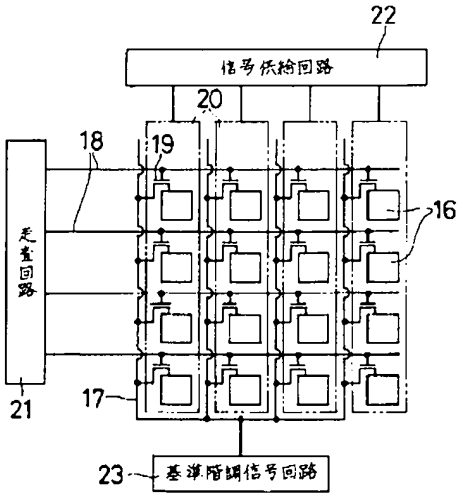
【図１７】



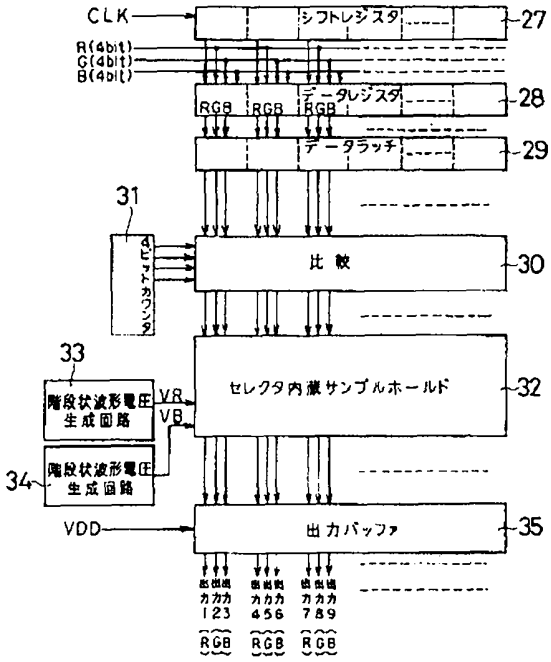
【図１８】



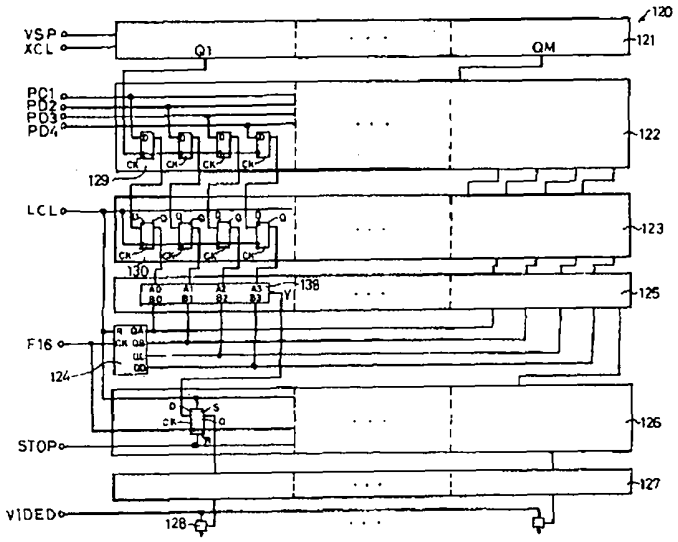
【図１９】



【図20】


CLK
シフトレジスタ
27
R(4bit)
G(4bit)
B(4bit)
データレジスタ
RGB
28
データラッチ
29
31
比較
30
33
階段状波形電圧生成回路
VR
VB
セレクタ内蔵サンプルホールド
32
34
階段状波形電圧生成回路
VDD
出力バッファ
35
RGB
RGB
RGB

【図21】


120
VSP
XCL
Q1
QM
121
PD1
PD2
PD3
PD4
122
129
LCL
123
130
138
125
F16
124
126
STOP
127
VIDEO
128

【図22】